IN THE SPECIFICATION

1.   **Please replace the paragraph on page 7 beginning at line 4 with the following paragraph:**

Figure 1 is a diagram illustrating a preferred embodiment of a portable electronic device 60, such as a portable digital music system, that may include the power management system in accordance with the invention. In this embodiment, the device shown has been implemented as a two processor system of a chip, but the power management system is applicable to any type of electronic device. The system may also include as a cross bar multipath memory controller 62 and a cross bar multipath peripheral controller 64 which are described in more detail in copending patent application serial number ~~09/XXX,XXX~~ 09/847,991 filed on ~~XXXXXXXX~~ May 2, 2001 and entitled "Cross Bar Multipath Resource Controller System and Method" which is owned by the same assignee as the present invention and which is incorporated herein by reference.

2.   **Please replace the paragraph on page 7 beginning at line 13 with the following new paragraph:**

As shown, the multiple processor system 60 may include a host processor 66 which may preferably be a reduced instruction set (RISC) ARM core made by ARM Inc and a coprocessor core 68 that operate in a cooperative manner to complete tasks as described above. In the preferred embodiment, there may also be a hardware accelerator engine 70 as shown. A software DMA engine 71 in this preferred embodiment may be executed by the coprocessor core 68. The software DMA engine is described in more detail in copending patent application serial number ~~09/XXX,XXX~~ 09/847,981 filed on ~~XXXXXXXX~~ May 2, 2001 and entitled

"Software Direct Memory Access Engine for Multiple Processor Systems" which is owned by the same assignee as the present invention and which is incorporated herein by reference.

3.   Please replace the paragraph on pages 7 and 8, beginning on Page 7 at line 22 with the following new paragraph:

In more detail, the host processor, the coprocessor and the hardware accelerator engine are all connected to the multipath memory controller 62 and the multipath peripheral controller 64 as shown which permit the host processor and the coprocessor to access each shared resource using its own bus. To control access to the shared resources connected to the multipath memory controller and the multipath peripheral controller, the system 60 may include a semaphore unit 72 which permits the two processors 66, 68 to communicate with each other and control the access to the shared resources. The details of the semaphore unit is described in more detail in copending US patent application number ~~XX/XXX,XXX~~ 09/847,976 filed on ~~XXXX,XX2001~~ May 2, 2001 titled "Multiprocessor Communications System and Method", owned by the same assignee as the present invention and incorporated herein by reference. The semaphore unit permits the processors to negotiate for the access to the shared resources as described above, but then, due to the multipath controllers 62, 64, permits the processors to access the resources over its own bus that is part of the controllers. To control the timing of the controllers 62, 64, a timer/clock 74 is connected to each controller 62, 64.

4.   Please replace the paragraph on page 13 beginning at line 10 with the following new paragraph:

The flexible clock generator 140 may also include a 16 bit PING LFSR 158 which is a random number generator (a preferred random number generator is described in co-pending patent application number ~~09/XXX,XXX~~ 09/847,982 filed ~~XXXX~~ May 2, 2001 and titled ~~"XXX"~~ "Random Number Generation Method and System" which is incorporated herein by reference), a us Timer 160 that generates as usTicks signal (this is a micro-second time pulse generator for various timing control) and a real-time clock and calendar (RTC) element 162. The real-time clock and calendar element may receive the 32 KHz clock signal as an input that is fed into a 5-bit prescalar 164, a 6 bit prescalar 166, a 6 bit prescalar 168 and a 15 bit prescalar 170 that are used to generate the real-time time and date for the system. In particular, one prescalar generates a day (Days) output, one prescalar generates a hours (Hrs) out put, one generates a minutes (Min) output and one generates a seconds (Sec) output as is well known.